WHAT IS CLAIMED IS:

1. A system for building a test case operable to test a circuit design, comprising:

an instruction generation engine for generating a set of instructions, at least one of said instructions including a temporarily uncommitted value;

a first summary generation engine portion for generating an interfaceable enumeration of said set of instructions, wherein each of said temporarily uncommitted values is denoted by an uncommitted reference; and

a second summary generation engine portion for resolving respective values of said uncommitted references and generating an interfaceable listing of said uncommitted references and their said respective values,

wherein said set of instructions and a summary including said interfaceable listing of said uncommitted references with resolved values are arranged to form said test case.

2. The system as recited in claim 1, wherein said temporarily uncommitted value relates to a data value at an address location.

3. The system as recited in claim 1, wherein said temporarily uncommitted value relates to an address location.

4. The system as recited in claim 1, wherein said set of instructions includes operations selected from the group consisting of loads, stores, and arithmetic operations.

5. The system as recited in claim 1, wherein said summary further includes said interfaceable enumeration of said set of instructions, each of said temporarily uncommitted values being denoted by an uncommitted reference.

6. The system as recited in claim 1, wherein said first summary generation engine portion generates said interfaceable enumeration as said instruction generation engine generates said set of instructions.

7. The system as recited in claim 1, wherein said instructions are operable to exercise a register-transfer level (RTL) model of an integrated circuit.

8. The system as recited in claim 1, wherein said instructions are operable to exercise an architectural simulation model of an integrated circuit.

9. The system as recited in claim 1, wherein said second summary generation engine portion resolves said respective values by recursively solving for said uncommitted references.

10. The system as recited in claim 1, wherein said second summary generation engine portion resolves said respective values by assigning a value to said uncommitted references.

11. The system as recited in claim 1, wherein said first and second summary generation engine portions are implemented in a software language selected from the group consisting of C, C++, and Perl.

12. A method for building a test case operable to test a circuit design, comprising:

generating a set of instructions, at least one of said instructions including an expression having a temporarily uncommitted value;

generating an interfaceable enumeration of said set of instructions, wherein each of said temporarily uncommitted values is denoted by an uncommitted reference;

resolving respective values of said uncommitted references;

generating an interfaceable listing of said uncommitted references and their said respective values; and

associating said set of instructions with said interfaceable enumeration of said set of instructions and said interfaceable listing of resolved uncommitted references, thereby forming said test case.

13. The method as recited in claim 12, wherein said operation of generating an interfaceable enumeration of said set of instructions occurs substantially simultaneously with said operation of generating a set of instructions.

14. The method as recited in claim 12, wherein said operation of resolving respective values of said uncommitted references further comprises recursively solving said uncommitted references.

15. The method as recited in claim 12, wherein said operation of resolving respective values of said uncommitted references further comprises assigning a value to said uncommitted references.

16. The method as recited in claim 12, further comprising utilizing said interfaceable listing in a debugging operation.

17. A computer-readable medium operable with a computer platform to build a test case for testing a circuit design, the medium having stored thereon:

program code for generating a set of instructions, at least one of said instructions including an expression having a temporarily uncommitted value;

program code for generating an interfaceable enumeration of said set of instructions, wherein each of said temporarily uncommitted values is denoted by an uncommitted reference;

program code for resolving respective values of said uncommitted references;

program code for generating an interfaceable listing of said uncommitted references and their said respective values; and

program code for associating said set of instructions with said interfaceable enumeration of said set of instructions and said interfaceable listing of resolved uncommitted references.

18. The computer-readable medium as recited in claim 17, wherein said program code for generating an interfaceable enumeration of said set of instructions is executed substantially simultaneously with said program code for generating a set of instructions.

19. The computer-readable medium as recited in claim 17, wherein said program code for resolving respective values of said uncommitted references further comprises program code for recursively solving said uncommitted references.

20. The computer-readable medium as recited in claim 17, wherein said program code for resolving respective values of said uncommitted references further comprises program code for assigning a value to said uncommitted references.

21. A computer system operable to simulate a platform for testing a circuit design, the computer system comprising:

a random number generator, operating responsive to a seed, for generating a random number sequence;

an event probability generator, operating responsive to profile settings, for generating a probability profile; and

a test generator, operating responsive to said random number sequence and said probability profile, for generating a test case including a set of instructions and an interfaceable summary of said set of instructions,

wherein said set of instructions includes at least one expression having a temporarily uncommitted value that is resolved by said test generator and presented in said interfaceable summary.

22. The computer system as recited in claim 21, wherein said test case is operable to exercise a register-transfer level (RTL) model of an integrated circuit.

23. The computer system as recited in claim 21, wherein said test case is operable to exercise an architectural simulation model of an integrated circuit.

24. The computer system as recited in claim 21, wherein said test generator is implemented in a software language selected from the group consisting of C, C++, and Perl.

25. The computer system as recited in claim 21, wherein said temporarily uncommitted value relates to a data value at an address location.

26. The computer system as recited in claim 21, wherein said temporarily uncommitted value relates to an address location.

27. A system for building a test case operable to test a circuit design, comprising:

means for generating a set of instructions, at least one of said instructions including an expression having a temporarily uncommitted value;

means for generating an interfaceable enumeration of said set of instructions, wherein each of said temporarily uncommitted values is denoted by an uncommitted reference;

means for resolving respective values of said uncommitted references;

means for generating an interfaceable listing of said uncommitted references and their said respective values; and

means for associating said set of instructions with said interfaceable enumeration of said set of instructions and said interfaceable listing of resolved uncommitted references, thereby forming said test case.